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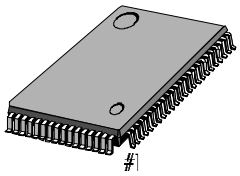
Jameco Part Number 151933



## INTRODUCTION

KS0066U is a dot matrix LCD driver & controller LSI whichis fabricated by low power CMOS technology.
It can display 1or 2 lines with the 5×8 dots format or 1 line with the 5×11 dots format.

80 QFP-1420C



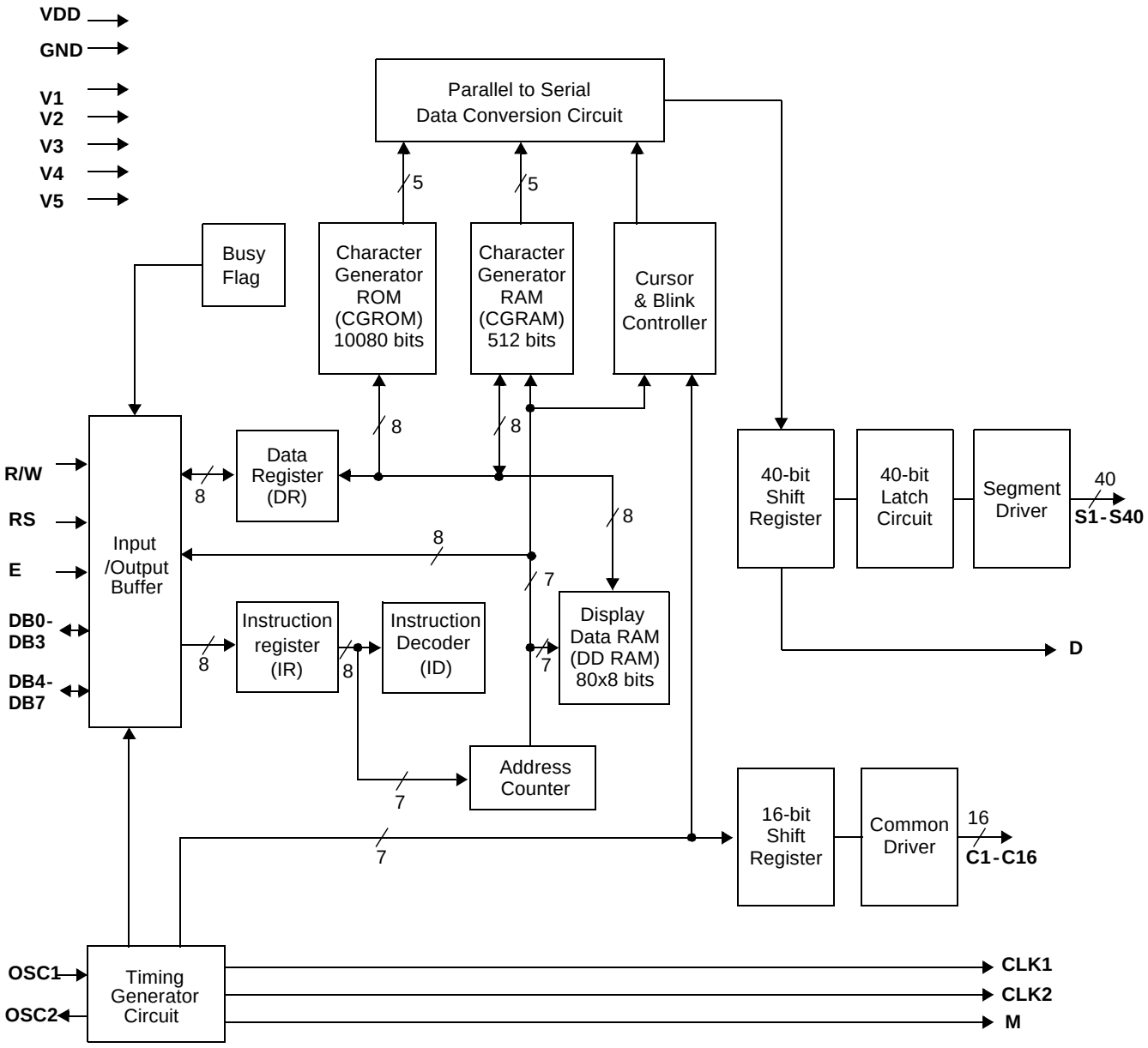
## FUNCTIONS

- Character type dot matrix LCD driver & controller.
- Internal driver: 16 common and 40 segment signal output.
- Easy interface with 4-bit or 8-bit MPU.
- Display character pattern: 5×8 dots format (208 kinds) & 5×11 dots format (32 kinds).
- The Special character pattern is directly programmable by the Character Generator RAM.
- A customer character pattern is programmable by mask option.
- Programmable Driving Method by the same character font mask option: Display Waveform A-type and B-type
- It can drive a maximum at 80 characters by using the KS0065B or KS0063B externally.
- Various instruction functions.
- Built-in automatic power on reset.

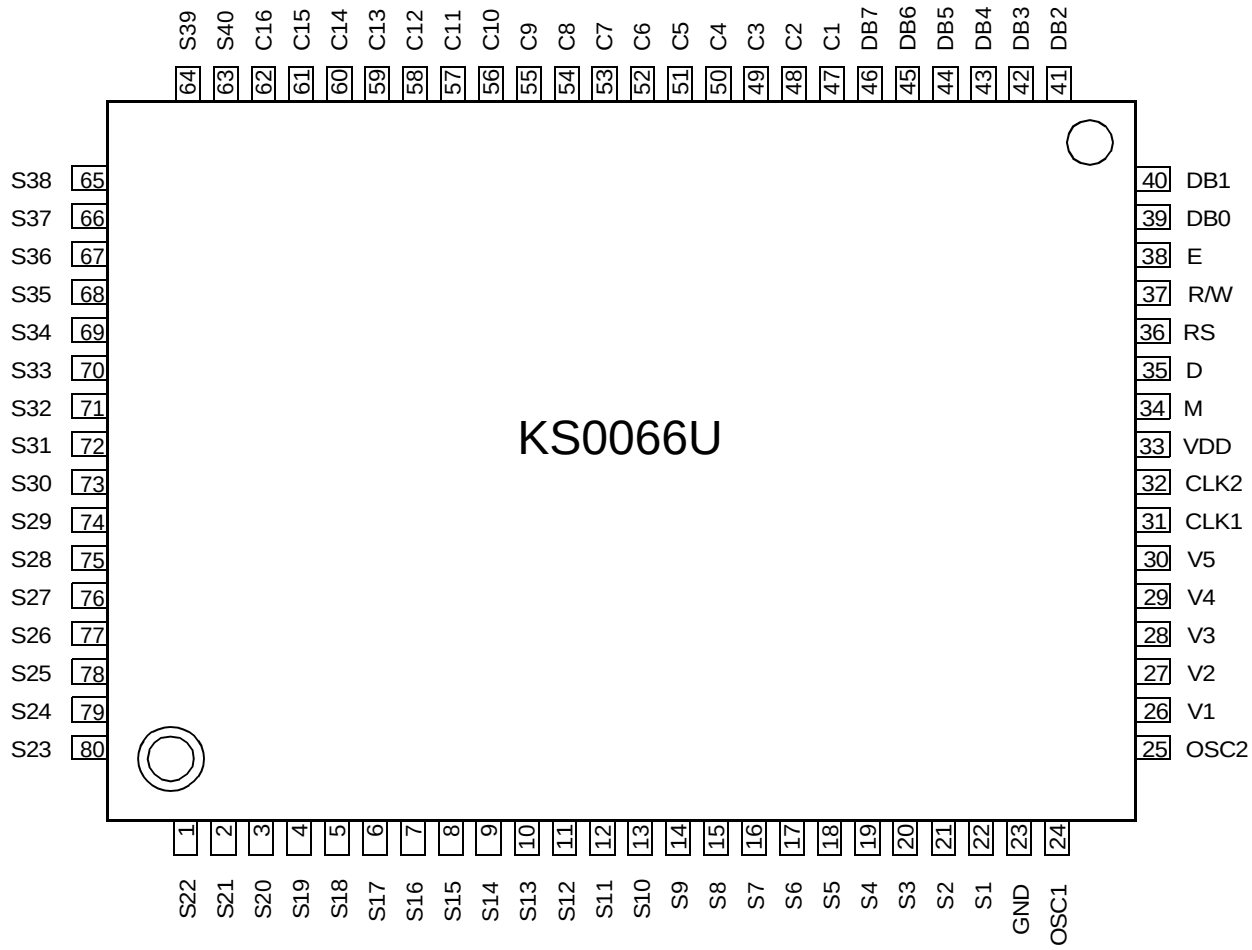
## FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 10,080 bits (204 characters×5×8 dots) & (32 characters×5×11 dots)
  - Character Generator RAM (CGRAM): 64×8 bits (8 characters×5×8 dots)
  - Display Data RAM (DDRAM): 80×8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range (VDD): 2.7 to 5.5 V
  - LCD Drive voltage range (VDD–V5): 3.0 to 13.0 V
- CMOS process
- Programmable duty cycle: 1/8, 1/11, 1/16
- Internal oscillator with external resistor
- Low power consumption
- 80 QFP or bare chip available

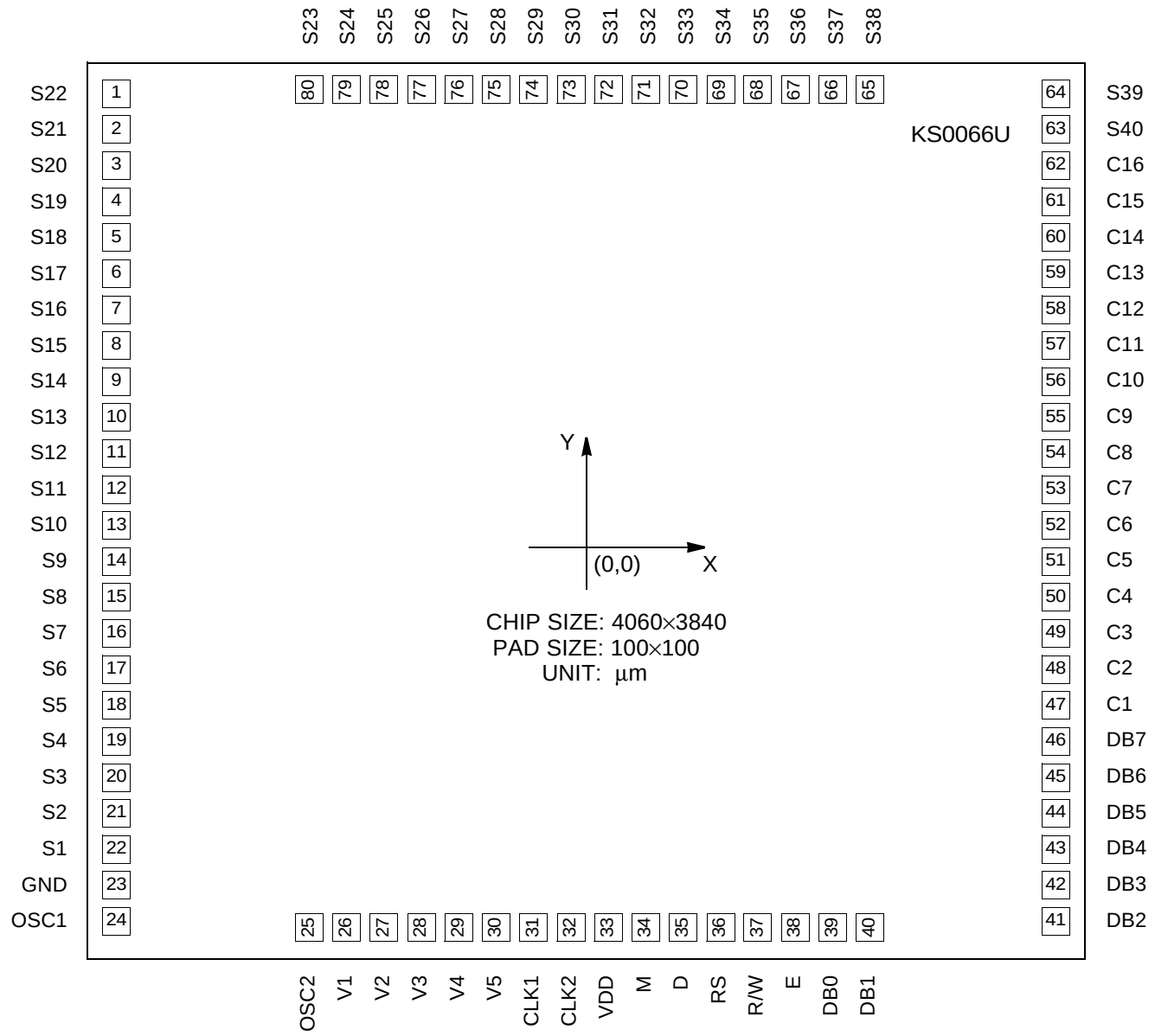
## BLOCK DIAGRAM



**PIN CONFIGURATION**



## PAD DIAGRAM




NOTE: “KS0066U” marking is to make the PAD No. 65 easy to find.

## PAD LOCATION

**Table 1. Pad Location**

**(Unit: ㎜)**

| Pad No. | Pad Name | Coordinate | | Pad No. | Pad Name | Coordinate | | Pad No. | Pad Name | Coordinate | | Pad No. | Pad Name | Coordinate | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | X | Y | | | X | Y | | | X | Y | | | X | Y |
| 1 | S22 | -1864 | 1465 | 21 | S2 | -1864 | -1034 | 41 | DB2 | 1864 | -1488 | 61 | C15 | 1864 | 1085 |
| 2 | S21 | -1864 | 1340 | 22 | S1 | -1864 | -1159 | 42 | DB3 | 1864 | -1362 | 62 | C16 | 1864 | 1210 |
| 3 | S20 | -1864 | 1215 | 23 | GND | -1864 | -1285 | 43 | DB4 | 1864 | -1238 | 63 | S40 | 1864 | 1341 |
| 4 | S19 | -1864 | 1090 | 24 | OSC1 | -1864 | -1414 | 44 | DB5 | 1864 | -1112 | 64 | S39 | 1864 | 1466 |
| 5 | S18 | -1864 | 965 | 25 | OSC2 | -1120 | -1754 | 45 | DB6 | 1864 | -988 | 65 | S38 | 886 | 1754 |
| 6 | S17 | -1864 | 840 | 26 | V1 | -970 | -1754 | 46 | DB7 | 1864 | -862 | 66 | S37 | 760 | 1754 |
| 7 | S16 | -1864 | 715 | 27 | V2 | -820 | -1754 | 47 | C1 | 1864 | -665 | 67 | S36 | 636 | 1754 |
| 8 | S15 | -1864 | 590 | 28 | V3 | -670 | -1754 | 48 | C2 | 1864 | -540 | 68 | S35 | 510 | 1754 |
| 9 | S14 | -1864 | 465 | 29 | V4 | -520 | -1754 | 49 | C3 | 1864 | -415 | 69 | S34 | 386 | 1754 |
| 10 | S13 | -1864 | 340 | 30 | V5 | -370 | -1754 | 50 | C4 | 1864 | -290 | 70 | S33 | 260 | 1754 |
| 11 | S12 | -1864 | 215 | 31 | CLK1 | -220 | -1754 | 51 | C5 | 1864 | -165 | 71 | S32 | 136 | 1754 |
| 12 | S11 | -1864 | 90 | 32 | CLK2 | -70 | -1754 | 52 | C6 | 1864 | -40 | 72 | S31 | 10 | 1754 |
| 13 | S10 | -1864 | -35 | 33 | VDD | 80 | -1754 | 53 | C7 | 1864 | 85 | 73 | S30 | -114 | 1754 |
| 14 | S9 | -1864 | -160 | 34 | M | 230 | -1754 | 54 | C8 | 1864 | 210 | 74 | S29 | -240 | 1754 |
| 15 | S8 | -1864 | -285 | 35 | D | 380 | -1754 | 55 | C9 | 1864 | 335 | 75 | S28 | -364 | 1754 |
| 16 | S7 | -1864 | -410 | 36 | RS | 518 | -1754 | 56 | C10 | 1864 | 460 | 76 | S27 | -490 | 1754 |
| 17 | S6 | -1864 | -535 | 37 | R/W | 642 | -1754 | 57 | C11 | 1864 | 585 | 77 | S26 | -614 | 1754 |
| 18 | S5 | -1864 | -660 | 38 | E | 768 | -1754 | 58 | C12 | 1864 | 710 | 78 | S25 | -740 | 1754 |
| 19 | S4 | -1864 | -785 | 39 | DB0 | 894 | -1754 | 59 | C13 | 1864 | 835 | 79 | S24 | -864 | 1754 |
| 20 | S3 | -1864 | -910 | 40 | DB1 | 1018 | -1754 | 60 | C14 | 1864 | 960 | 80 | S23 | -989 | 1754 |

## PIN DESCRIPTION

**Table 2. Pin Description**

| Pin | Pin No. | I/O | Name | Description | Interface |
|---|---|---|---|---|---|
| VDD | 33 | - | Supply Voltage | Supply Voltage for logical circuit (+3V ± 10%,+5V ± 10%) | Power Supply |
| GND | 23 | | | Ground (0V) | |
| V1-V5 | 26-30 | | | Bias voltage level for LCD driving | |
| S1-S40 | 1-22, 63-80 | O | Segment output | Segment signal output for LCD drive | LCD |
| C1-C16 | 47-62 | O | Common output | Common signal output for LCD drive | LCD |
| OSC1 | 24 | I | Oscillator | Oscillator. When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1. | External resistor/oscillator (OSC1) |
| OSC2 | 25 | O | Oscillator | | |
| CLK1 | 31 | O | Extension driver Latch clock | Extension driver latch clock | Extension driver |
| CLK2 | 32 | O | Extension driver Shift clock | Extension driver shift clock | |
| M | 34 | O | Alternated signal for LCD driver output | Outputs the alternating signal to convert LCD driver waveform to AC. | Extension driver |
| D | 35 | O | Display data interface | Outputs extension driver data (the 41st dot's data) | Extension driver |
| RS | 36 | I | Register select | Used as register selection input.<br>When RS = "High", Data register is selected.<br>When RS = "Low", Instruction register is selected. | MPU |
| R/W | 37 | I | Read/Write | Used as read/write selection input.<br>When RW = "High", read operation.<br>When RW = "Low", write operation. | MPU |
| E | 38 | I | Read/Write enable | Used as read/write enable signal. | MPU |
| DB0-DB3 | 39-42 | I/O | Data bus 0-7 | In 8-bit bus mode, used as low order bidirectional data bus.<br>In 4-bit bus mode, open these pins. | MPU |
| DB4-DB7 | 43-46 | | | In 8-bit bus mode, used as high order bidirectional data bus.<br>In 4-bit bus mode, used as both high and low order.<br>DB7 used for Busy Flag output. | MPU |

## FUNCTION DESCRIPTION

### System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used.
One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction.
Each internal operation, reading from or writing into RAM, is done automatically.
Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction codes transferred from MPU.
MPU cannot use it to read instruction data.

To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

**Table 3. Various kinds of Operations according to RS and R/W bits**

| RS | R/W | Operation |
|---|---|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy flag(DB7) and address counter (DB0 to DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

### Busy Flag (BF)

BF = "High", indicates that the internal operation is being processed.
So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = "Low" and R/W = "High" (Read Instruction Operation).
Before executing the next instruction, be sure that BF is not "High".

### Address Counter (AC)

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through ports DB0 to DB6.

**Display Data RAM (DDRAM)**

DDRAM stores display data of maximum 80×8 bits (80 characters).
DDRAM address is set in the address counter(AC) as a hexadecimal number (Refer to Fig-1.)

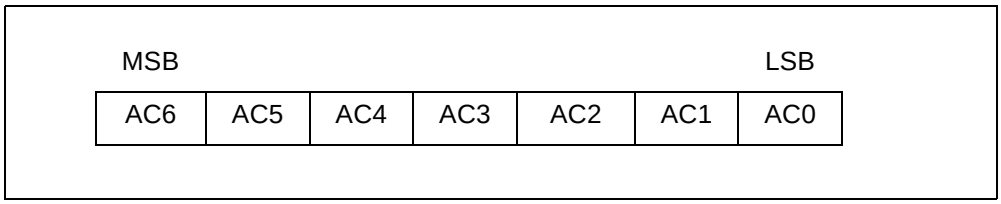



**Figure 1 . DDRAM Address**

1) 1-line display
In case of 1-line display, the address range of DDRAM is 00H–4FH.
An extension driver will be used. Fig-2 shows the example with 40 segment extension driver added.

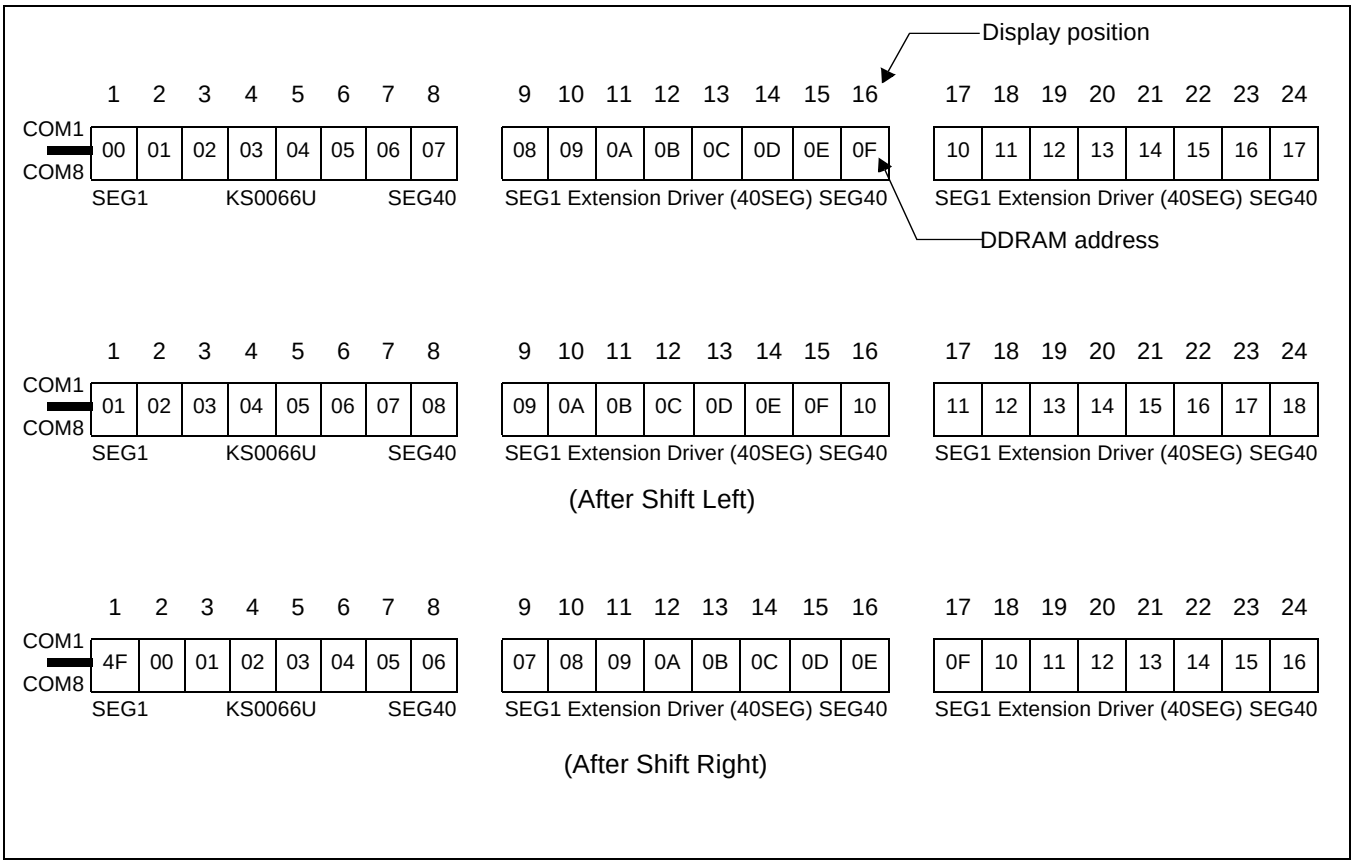



**Figure 2 . 1-line ´ 24 char. display with 40 SEG. extension driver**

2) 2-line display

In case of 2-line display, the address range of DDRAM is 00H–27H and 40H–67H.
An extension driver will be used. Fig-3 shows the example with 40 segment extension driver added.

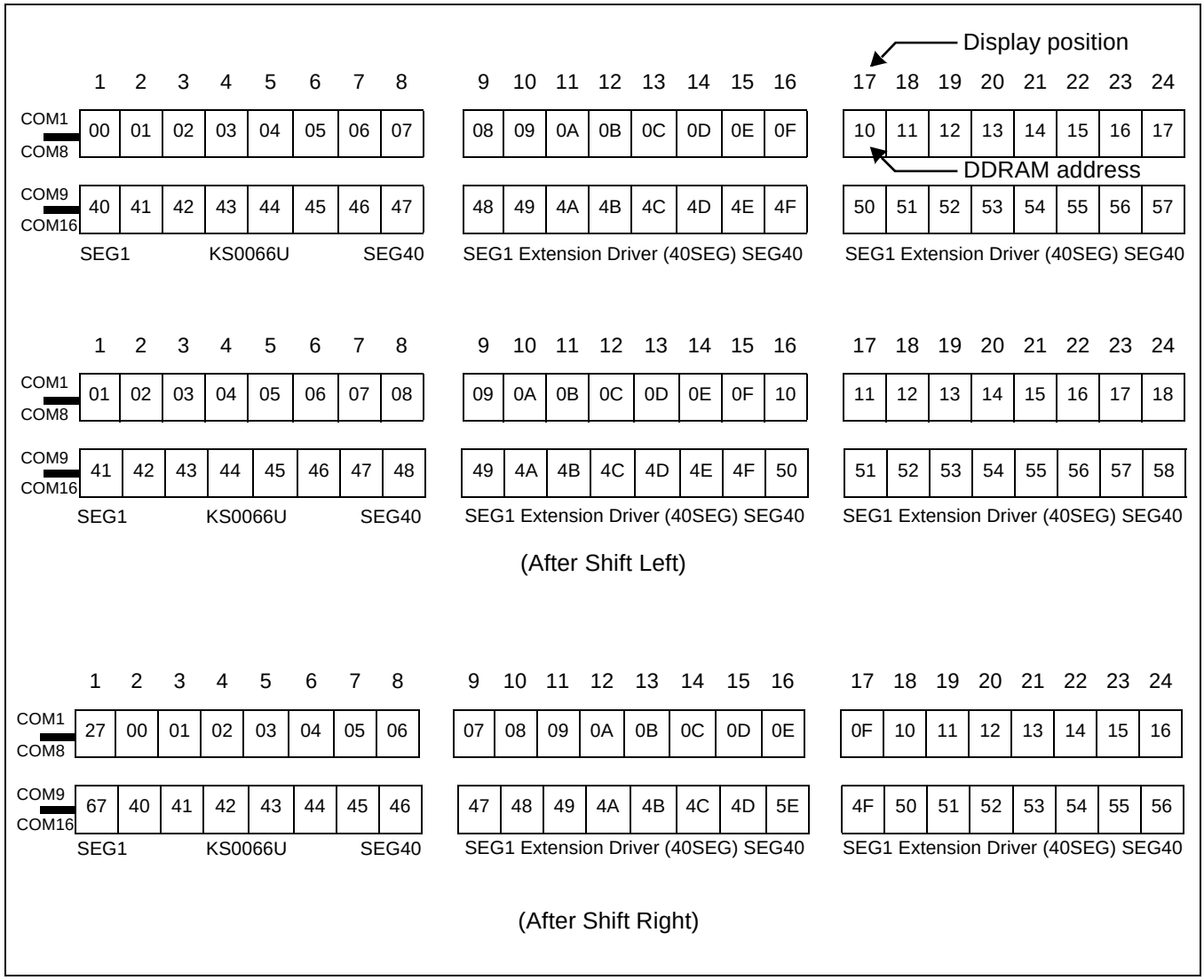



**Figure 3 . 2-line ´ 24 char. display with 40 SEG. extension driver**

**CGROM(Character Generator ROM)**

CGROM has a 5×8 dots 204 characters pattern and a 5×11 dots 32 characters pattern (Refer to Table 4).
CGROM has 204 character patterns of 5× 8 dots, and 32 character patterns of 5×11 dots.

**CGRAM(Character Generator RAM)**

CGRAM has up to 5×8 dots 8 characters.
By writing font data to CGRAM, user defined characters can be used (Refer to Table 5)

**Timing Generation Circuit**

Timing generation circuit generates clock signals for the internal operations.

**LCD Driver Circuit**

LCD Driver circuit has 16 common and 40 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to a 40-bit segment latch serially, and then is stored to 40-bit shift latch.
When each common is selected by 16-bit common register, segment data is also output through segment driver from a 40-bit segment latch.
In case of 1-line display mode, COM1 to COM8 have 1/8 duty or COM1 to COM11 have 1/11 duty,
and in 2-line mode, COM1 to COM16 have a 1/16 duty ratio.

**Cursor/Blink Control Circuit**

It controls the cursor/blink ON/OFF at cursor position.

**Table 4. CGROM Character Code Table**

**Table 5. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)**

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | | | CGRAM Data | | | | | | | | Pattern number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | |
| 0 | 0 | 0 | 0 | × | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | × | × | × | 0 | 1 | 1 | 1 | 0 | pattern 1 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 0 | × | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | × | × | × | 1 | 0 | 0 | 0 | 1 | pattern 8 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |

## INSTRUCTION DESCRIPTION

### Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control informations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 7).
Instructions can be divided largely into four groups:

1) KS0066U function set instructions (set display methods, set data length, etc.)
2) address set instructions to internal RAM
3) data transfer instructions with internal RAM
4) others

The address of the internal RAM is automatically increased or decreased by 1.

Note: During internal operation, Busy Flag (DB7) is read "High".
Busy Flag check must be preceded by the next instruction.
When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

### Contents

1) Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address,
and set DDRAM address to "00H" into AC (address counter).
Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.
Make the entry mode increment (I/D = "High").

2) Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |

* "-": dont care

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Entry Mode Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH |

Set the moving direction of cursor and display.

**I/D: Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

**SH: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or SH = "Low", shifting of entire display is not performed.
If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value
(I/D = "High": shift left, I/D = "Low": shift right).

4) Display ON/OFF Control

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

**D: Display ON/OFF control bit**
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data remains in DDRAM.

**C: Cursor ON/OFF control bit**
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register preserves its data.

**B: Cursor Blink ON/OFF control bit**
When B = "High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - |

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.(Refer to Table 6)
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

**Table 6. Shift Patterns According to S/C and R/L Bits**

| S/C | R/L | Operation |
|---|---|---|
| 0 | 0 | Shift cursor to the left, AC is decreased by 1 |
| 0 | 1 | Shift cursor to the right, AC is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

6) Function Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - |

**DL: Interface data length control bit**
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data twice.

**N: Display line number control bit**
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.

**F: Display font type control bit**
When F = "Low", 5 ×8 dots format display mode is set.
When F = "High", 5 ×11 dots format display mode.

7) Set CGRAM Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = Low), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = High), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether KS0066U is in internal operation or not.
If the resultant BF is "High", internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not Yet determined. If RAM data is read several times without RAM address instructions set before read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.
After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates the next address position, but only the previous data can be read by the read instruction.

**Table 7. Instruction Table**

| Instruction | Instruction Code | | | | | | | | | | Description | Execution time (fosc= 270 kHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM and set DDRAM address to "00H" from AC | 1.53 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.53 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction and enable the shift of entire display. | 39 µs |
| Display ON/ OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display(D), cursor(C), and blinking of cursor(B) on/off control bit. | 39 µs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | - | - | Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data. | 39 µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | - | - | Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5×11dots/5×8 dots) | 39 µs |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 39 µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 39 µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 µs |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM). | 43 µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM). | 43 µs |

* "-": dont care

NOTE: When an MPU program with checking the Busy Flag(DB7) is made, it must be necessary 1/2Fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "Low".

**INTERFACE WITH MPU**

1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below.

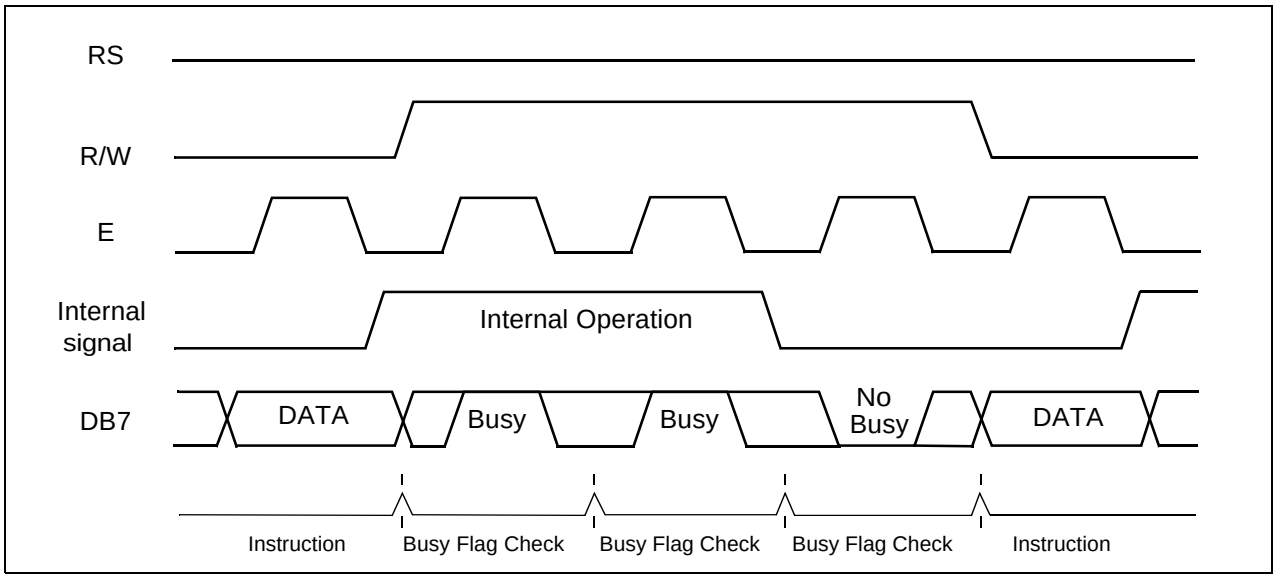



**Figure 4 . Example of 8-bit Bus Mode Timing Diagram**

2) Interface with 4-bit MPU

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At First, the higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7), and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed twice
Busy Flag outputs "High" after the second transfer is ended.
Example of timing sequence is shown below.

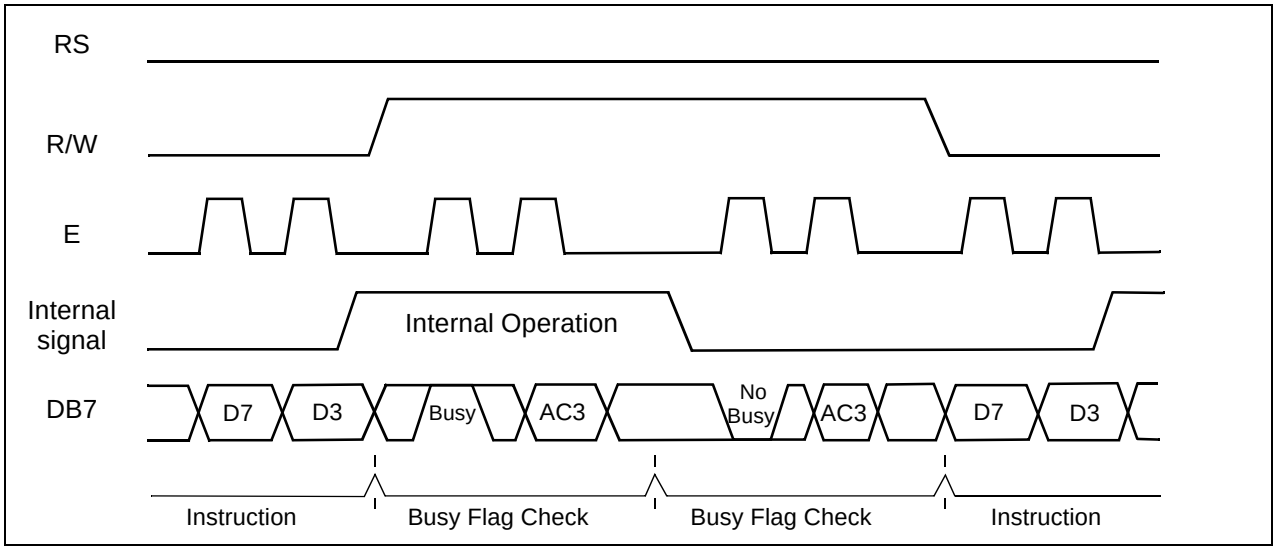
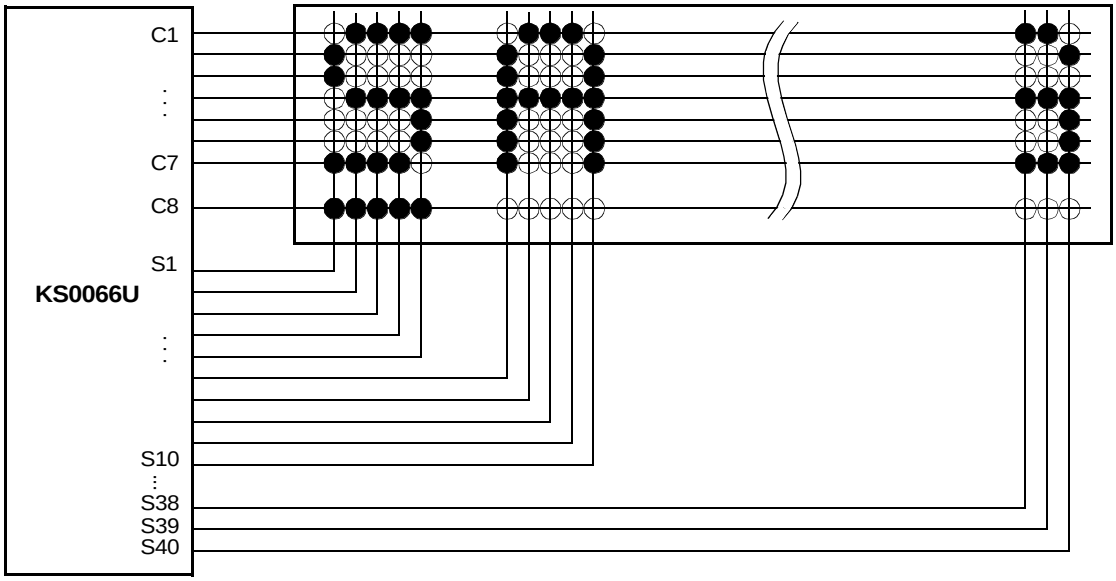


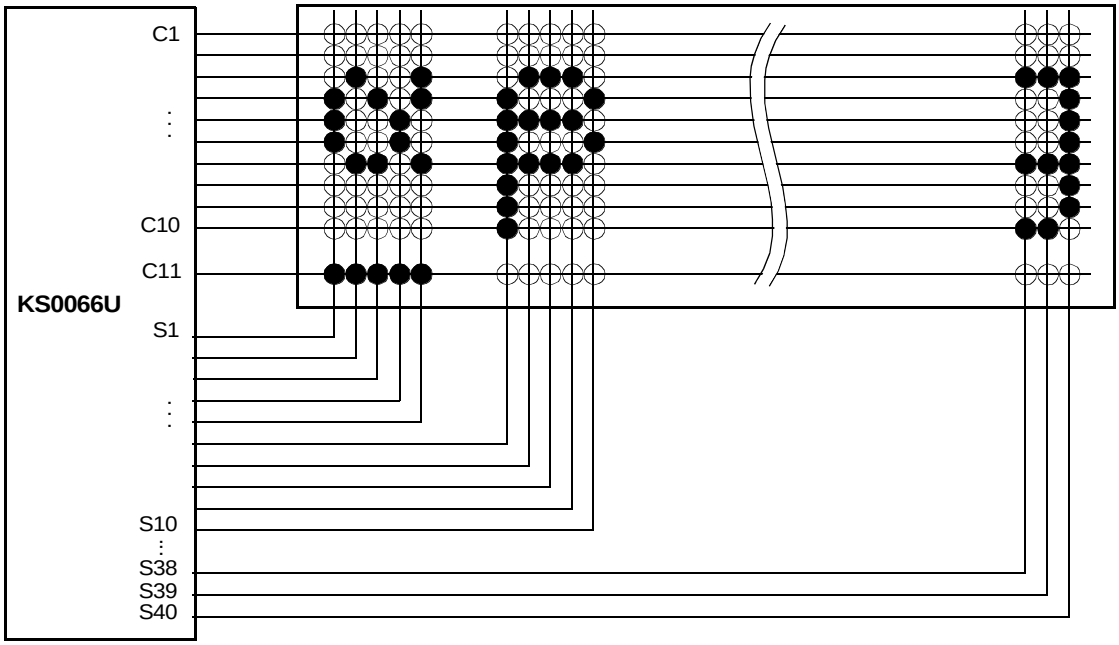

**Figure 5 . Example of 4-bit Bus Mode Timing Diagram**

## APPLICATION INFORMATION ACCORDING TO LCD PANEL

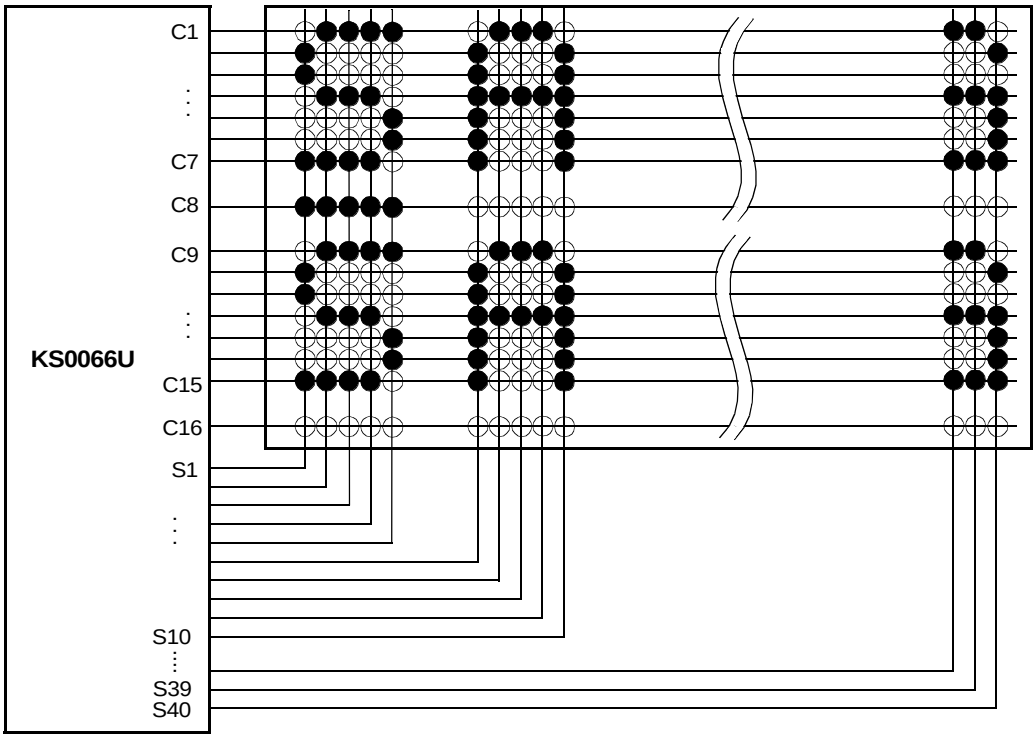
1) LCD Panel: 8 characters ×1-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



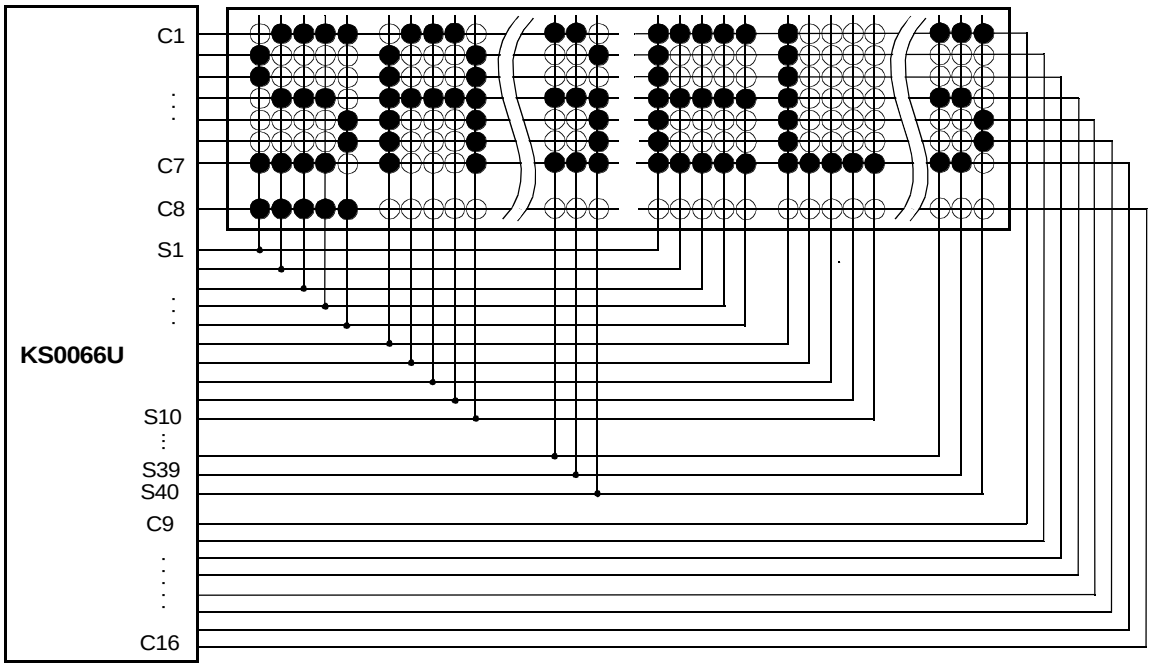

2) LCD Panel: 8 characters ×1-line format (5×10 dots + 1cursor line, 1/4 bias, 1/11 duty)



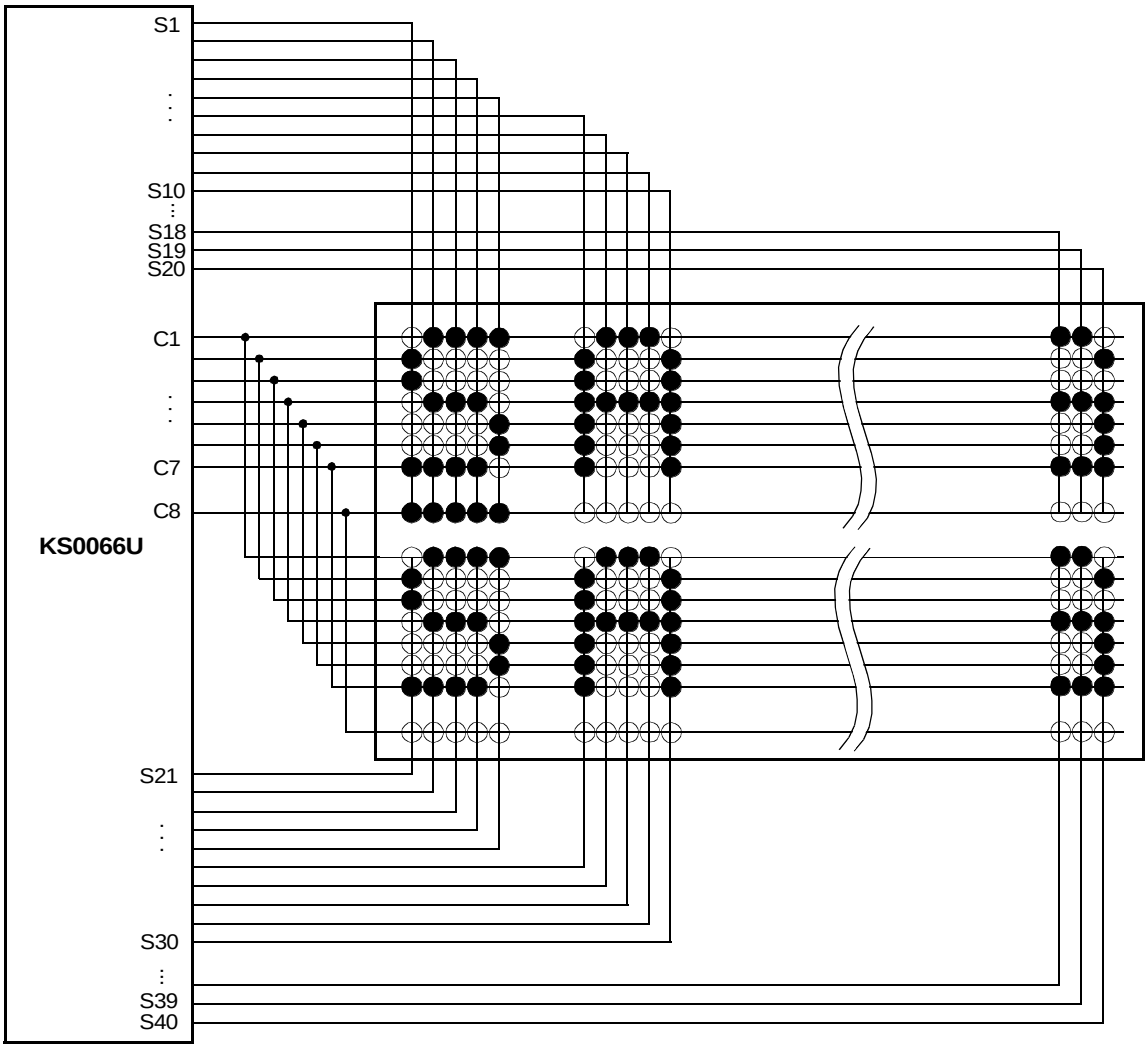
3) LCD Panel: 8 characters ×2 -line format (5×7 dots + line, 1/5 bias, 1/16 duty)



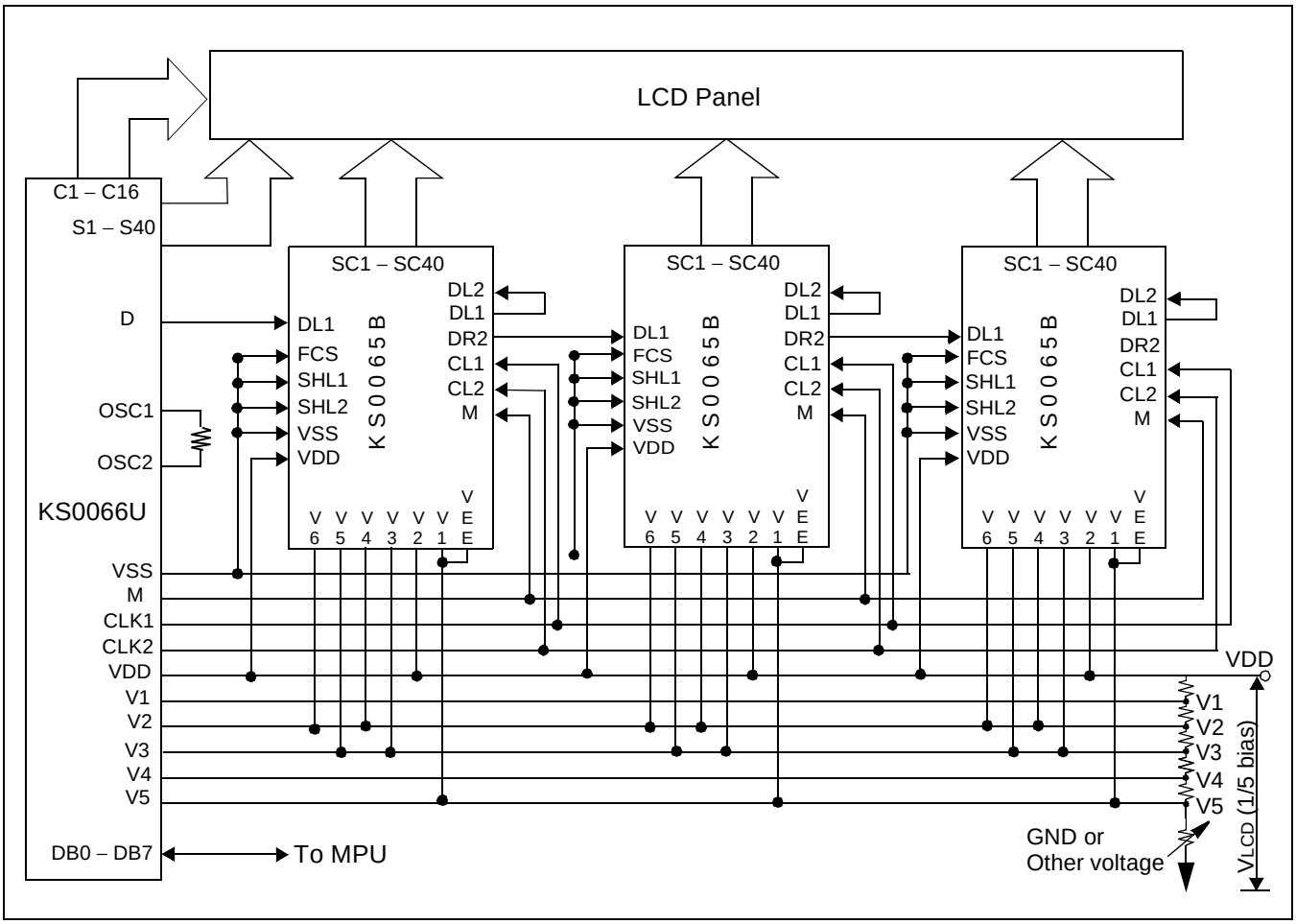

4) LCD Panel: 16 characters ×1-line format (5×7 dots + 1cursor line, 1/5 bias, 1/16 duty)



5) LCD Panel: 4 characters ×2-line format (5×7 dots + 1cursor line, 1/4 bias, 1/8 duty)



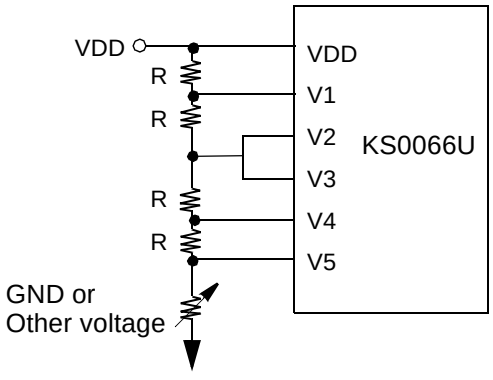
6) APPLICATION CIRCUIT



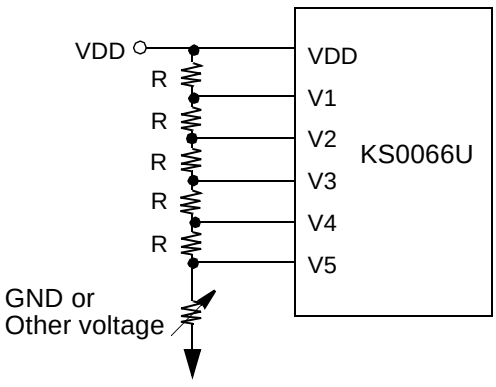

NOTE: When KS0065B is externally connected to the KS0066U, you can increase the number of display digits up to 80 characters.

**BIAS VOLTAGE DIVIDE CIRCUIT**

1) 1/4 bias, 1/8 or 1/11 duty




2) 1/5 bias, 1/16 duty



**INITIALIZING**

When the power is turned on, KS0066U is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High" (busy state) to the end of initialization.

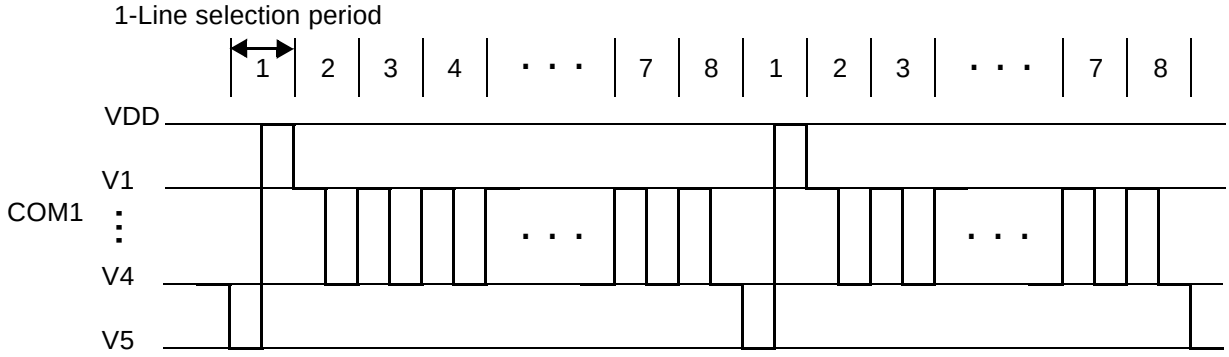
(1) Display Clear instruction: Write "20H" to all DDRAM
(2) Set Functions instruction: DL = "High": 8-bit bus mode
N = "Low": 1-line display mode
F = "Low": 5 X 8 font type
(3) Control Display ON/OFF instruction: D = "Low": Display OFF
C = "Low": Cursor OFF
B = "Low": Blink OFF
(4) Set Entry Mode instruction: I/D = "High": Increment by 1
SH = "Low": No entire display shift

**FRAME FREQUENCY**

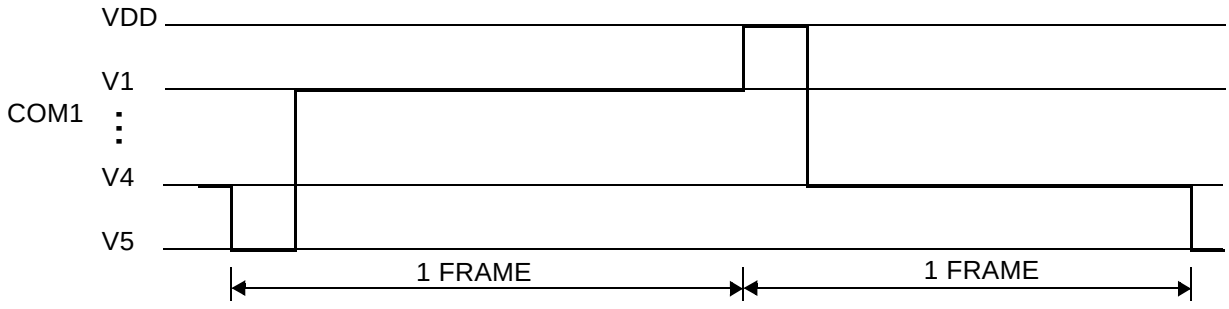
Programmable Driving Method by the same font mask option: Display waveform A-Type, B-Type

1) 1/8 duty cycle

A) A-type Waveform



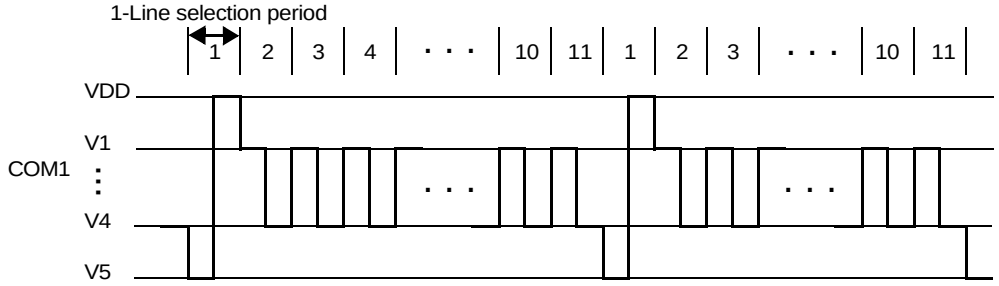

B) B-type Waveform



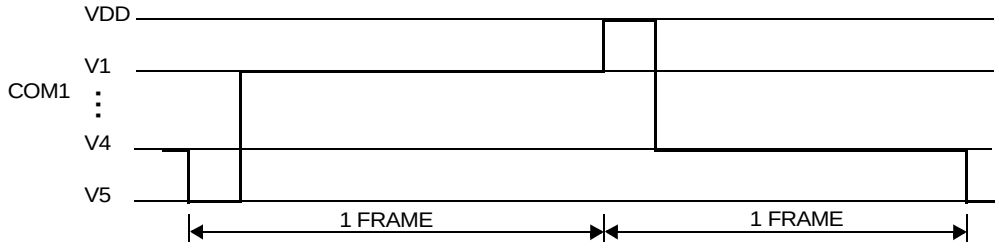

1-Line selection period = 400 clocks
1 Frame = 400×8×3.7 μs = 11850 μs = 11.9 ms (1 clock=3.7 μs, fosc=270 kHz)
Frame frequency = 1 / 11.9 ms = 84.4 Hz

2) 1/11 duty cycle

A) A-type Waveform



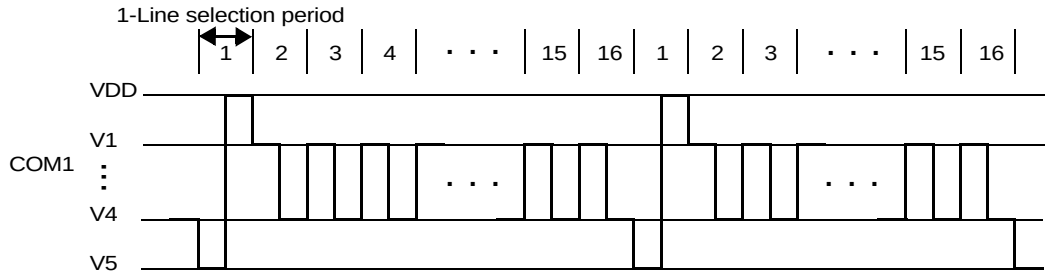

B) B-type Waveform



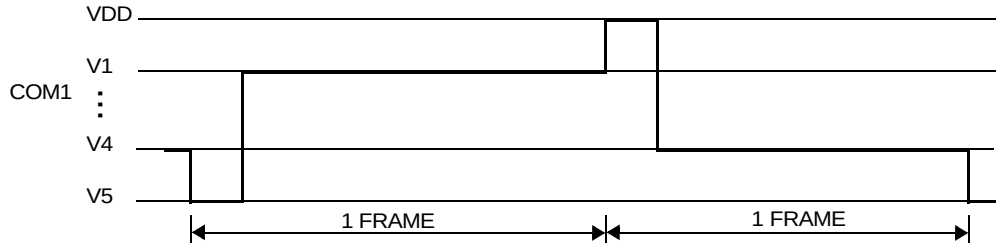

1-Line selection period = 400 clocks
1 Frame = 400×11×3.7 μs = 16300 μs = 16.3 ms (1 clock=3.7 μs, fosc=270 kHz)
Frame frequency = 1 / 16.3 ms = 61.4 Hz

3) 1/16 duty cycle

A) A-type Waveform



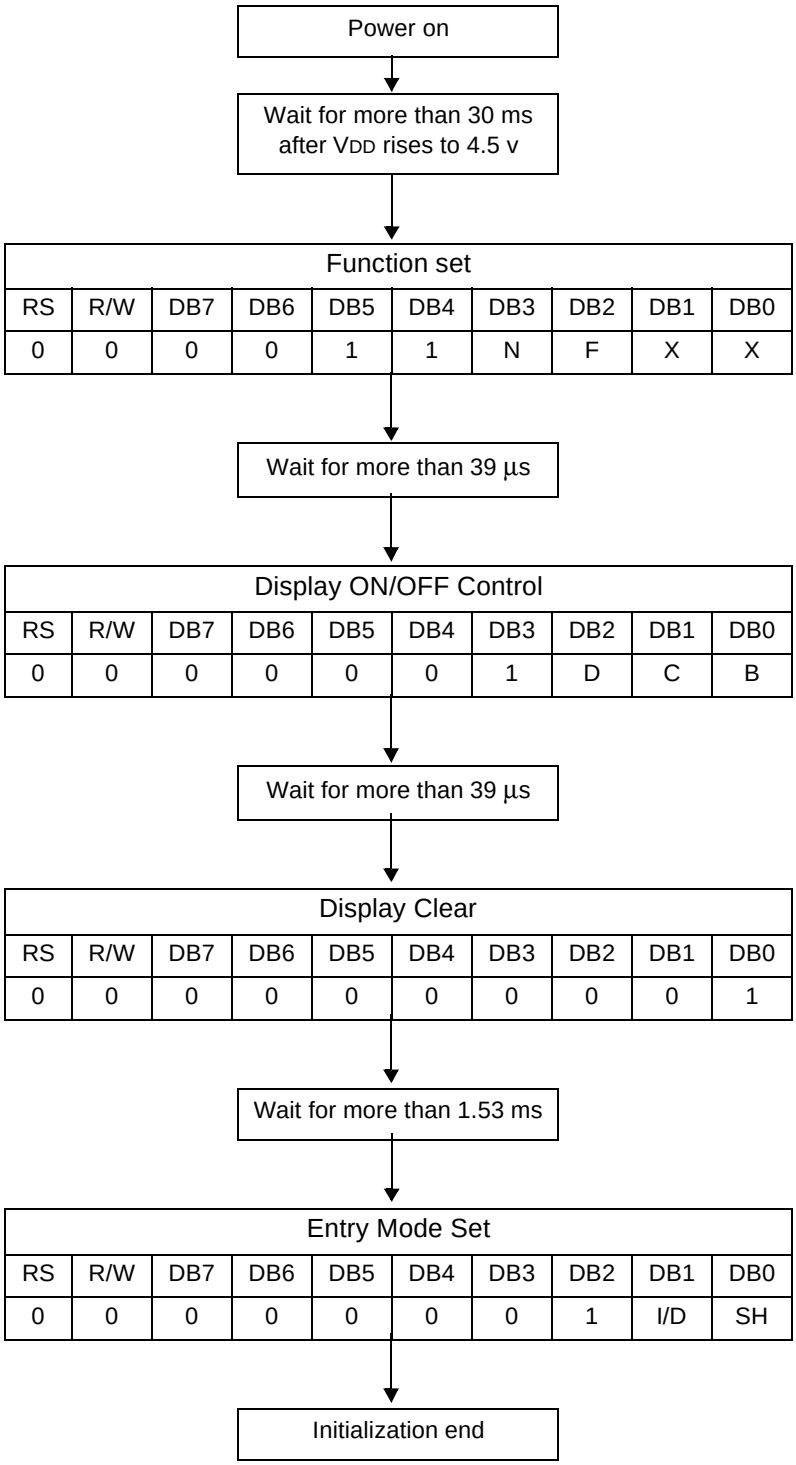

B) B-type Waveform




1-Line selection period = 200 clocks
1 Frame = 200×16×3.7 μs = 11850 μs = 11.9 ms (1 clock=3.7 μs, fosc=270 kHz)
Frame frequency = 1 / 11.9 ms = 84.3 Hz

**INITIALIZING BY INSTRUCTION**

1) 8-bit interface mode (Condition: fosc = 270KHZ)


Power on
Wait for more than 30 ms after VDD rises to 4.5 v
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 N F X X
Wait for more than 39 µs
Display ON/OFF Control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 1 D C B
Wait for more than 39 µs
Display Clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 0 0 1
Wait for more than 1.53 ms
Entry Mode Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 1 I/D SH
Initialization end

| | | |
|---|---|---|
| N | 0 | 1-line mode |
| | 1 | 2-line mode |

| | | |
|---|---|---|
| F | 0 | display off |
| | 1 | display on |

| | | |
|---|---|---|
| D | 0 | display off |
| | 1 | display on |

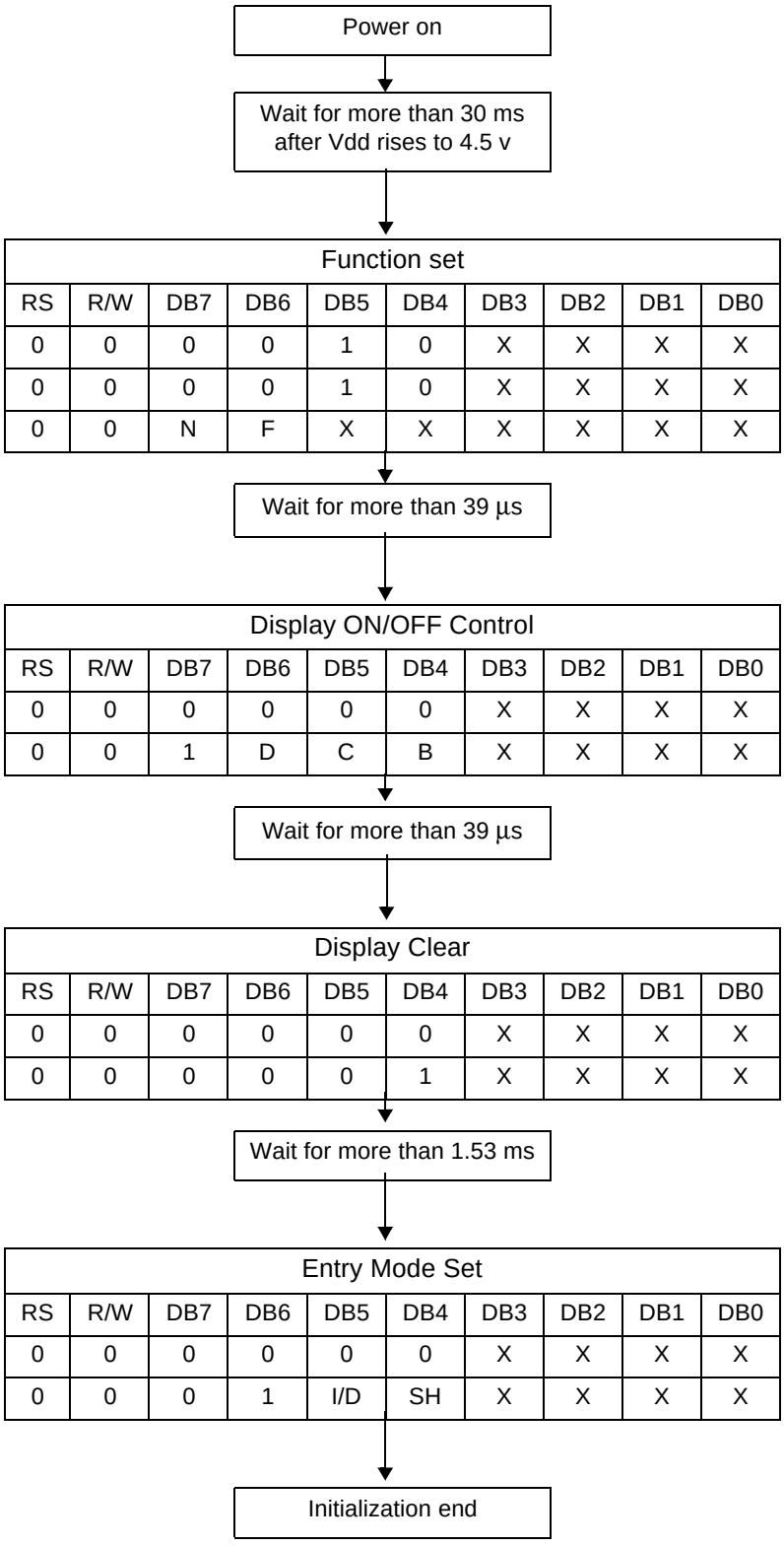
| | | |
|---|---|---|
| C | 0 | cursor off |
| | 1 | cursor on |

| | | |
|---|---|---|
| B | 0 | blink off |
| | 1 | blink on |

| | | |
|---|---|---|
| I/D | 0 | decrement mode |
| | 1 | increment mode |

| | | |
|---|---|---|
| SH | 0 | entire shift off |
| | 1 | entire shift on |

2) 4-bit interface mode (Condition: fosc = 270KHZ)


Power on
Wait for more than 30 ms after Vdd rises to 4.5 v
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 0 X X X X
0 0 0 0 1 0 X X X X
0 0 N F X X X X X X
Wait for more than 39 µs
Display ON/OFF Control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 1 D C B X X X X
Wait for more than 39 µs
Display Clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 0 0 1 X X X X
Wait for more than 1.53 ms
Entry Mode Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 1 I/D SH X X X X
Initialization end

| | | |
|---|---|---|
| N | 0 | 1-line mode |
| | 1 | 2-line mode |

| | | |
|---|---|---|
| F | 0 | display off |
| | 1 | display on |

| | | |
|---|---|---|
| D | 0 | display off |
| | 1 | display on |

| | | |
|---|---|---|
| C | 0 | cursor off |
| | 1 | cursor on |

| | | |
|---|---|---|
| B | 0 | blink off |
| | 1 | blink on |

| | | |
|---|---|---|
| I/D | 0 | decrement mode |
| | 1 | increment mode |

| | | |
|---|---|---|
| SH | 0 | entire shift off |
| | 1 | entire shift on |

## MAXIMUM ABSOLUTE LIMIT

**Table 8. Maximum Absolute Power Ratings**

| Characteristic | Symbol | Unit | Value |
|---|---|---|---|
| Power Supply Voltage(1) | $V_{DD}$ | V | -0.3 ~ +7.0 |
| Power Supply Voltage(2) | $V_{LCD}$ | V | $V_{DD}$-15.0 ~ $V_{DD}$+0.3 |
| Input Voltage | $V_{IN}$ | V | -0.3 ~ $V_{DD}$+0.3 |

NOTE: Voltage greater than above may damage the circuit.
$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

**Table 9. Temperature characteristics**

| Characteristic | Symbol | Unit | Value |
|---|---|---|---|
| Operating Temperature | $T_{OPR}$ | °C | -30 ~ +85 |
| Storage Temperature | $T_{STG}$ | °C | -55 ~ +125 |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

**Table 10. DC Characteristics ($V_{DD}$ = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)**

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 4.5 | - | 5.5 | V |
| Supply Current | $I_{DD}$ | Internal oscillation or external clock. ($V_{DD}$=5.0 V, fosc = 270 kHz) | - | 0.35 | 0.6 | mA |
| Input Voltage (1) (except OSC1) | $V_{IH1}$ | - | 2.2 | - | $V_{DD}$ | V |
| | $V_{IL1}$ | - | -0.3 | - | 0.6 | |
| Input Voltage (2) (OSC1) | $V_{IH2}$ | - | $V_{DD}$-1.0 | - | $V_{DD}$ | V |
| | $V_{IL2}$ | - | -0.2 | - | 1.0 | |
| Output Voltage (1) (DB0 to DB7) | $V_{OH1}$ | $I_{OH}$ = -0.205 mA | 2.4 | - | - | V |
| | $V_{OL1}$ | $I_{OL}$ = 1.2 mA | - | - | 0.4 | |
| Output Voltage (2) (except DB0 to DB7) | $V_{OH2}$ | $I_O$ = -40 μA | 0.9$V_{DD}$ | - | - | V |
| | $V_{OL2}$ | $I_O$ = 40 μA | - | - | 0.1$V_{DD}$ | |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1 mA | - | - | 1 | V |
| | $Vd_{SEG}$ | | - | - | 1 | |
| Input Leakage Current | $I_{IKG}$ | $V_{IN}$ = 0 V to $V_{DD}$ | -1 | - | 1 | μA |
| Input Low Current | $I_{IL}$ | $V_{IN}$ = 0 V, $V_{DD}$ = 5 V (PULL UP) | -50 | -125 | -250 | |
| Internal Clock (external Rf) | $f_{OSC1}$ | Rf = 91 kΩ ± 2% ($V_{DD}$ = 5 V) | 190 | 270 | 350 | kHz |
| External Clock | $f_{OSC}$ | - | 125 | 270 | 410 | kHz |
| | duty | | 45 | 50 | 55 | % |
| | $t_R$, $t_F$ | | - | - | 0.2 | μs |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$-$V_5$ (1/5, 1/4 Bias) | 3.0 | - | 13.0 | V |

**Table 11. DC Characteristic ($V_{DD}$ =2.7V ~ 4.5V, Ta = -30 ~ +85°C)**

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 2.7 | - | 4.5 | V |
| Supply Current | $I_{DD}$ | Internal oscillation or external clock. ($V_{DD}$=3.0 V, fosc = 270 kHz) | - | 0.15 | 0.3 | mA |
| Input Voltage (1) (except OSC1) | $V_{IH1}$ | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL1}$ | - | -0.3 | - | 0.55 | |
| Input Voltage (2) (OSC1) | $V_{IH2}$ | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL2}$ | - | - | - | $0.2V_{DD}$ | |
| Output Voltage (1) (DB0 to DB7) | $V_{OH1}$ | $I_{OH}$ = -0.1 mA | $0.75V_{DD}$ | - | - | V |
| | $V_{OL1}$ | $I_{OL}$ = 0.1 mA | - | - | $0.2V_{DD}$ | |
| Output Voltage (2) (except DB0 to DB7) | $V_{OH2}$ | $I_O$ = -40 µA | $0.8V_{DD}$ | - | - | V |
| | $V_{OL2}$ | $I_O$ = 40 µA | - | - | $0.2V_{DD}$ | |
| Voltage Drop | $Vd_{COM}$ | $I_O = \pm$ 0.1 mA | - | - | 1 | V |
| | $Vd_{SEG}$ | | - | - | 1 | |
| Input Leakage Current | $I_{IKG}$ | $V_{IN}$ = 0 V to $V_{DD}$ | -1 | - | 1 | µA |
| Input Low Current | $I_{IL}$ | $V_{IN}$ = 0 V, $V_{DD}$ = 3 V (PULL UP) | -10 | -50 | -120 | |
| Internal Clock (external Rf) | $f_{OSC1}$ | Rf = 75 kΩ $\pm$ 2% ($V_{DD}$ = 3 V) | 190 | 270 | 350 | kHz |
| External Clock | $f_{OSC2}$ | - | 125 | 270 | 410 | kHz |
| | duty | | 45 | 50 | 55 | % |
| | $t_R$,$t_F$ | | - | - | 0.2 | µs |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$-$V_5$ (1/5, 1/4 Bias) | 3.0 | - | 13.0 | V |

NOTE: LCD Driving Voltage

| Power | Duty | 1/8, 1/11 Duty | 1/16 Duty |
|---|---|---|---|
| | Bias | 1/4 Bias | 1/5 Bias |
| $V_{DD}$ | | $V_{DD}$ | $V_{DD}$ |
| $V_1$ | | $V_{DD}$-$V_{LCD}$/4 | $V_{DD}$-$V_{LCD}$/5 |
| $V_2$ | | $V_{DD}$-$V_{LCD}$/2 | $V_{DD}$-2$V_{LCD}$/5 |
| $V_3$ | | $V_{DD}$-$V_{LCD}$/2 | $V_{DD}$-3$V_{LCD}$/5 |
| $V_4$ | | $V_{DD}$-3$V_{LCD}$/4 | $V_{DD}$-4$V_{LCD}$/5 |
| $V_5$ | | $V_{DD}$-$V_{LCD}$ | $V_{DD}$-$V_{LCD}$ |

**AC Characteristics**

**Table 12. AC Characteristics ($V_{DD}$ = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)**

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Fig-6) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | $t_R$,$t_F$ | - | - | 20 | |
| | E Pulse Width (High, Low) | tw | 230 | - | - | |
| | R/W and RS Setup Time | tsu1 | 40 | - | - | |
| | R/W and RS Hold Time | $t_{H1}$ | 10 | - | - | |
| | Data Setup Time | tsu2 | 80 | - | - | |
| | Data Hold Time | $t_{H2}$ | 10 | - | - | |
| Read Mode (Refer to Fig-7) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | $t_R$,$t_F$ | - | - | 20 | |
| | E Pulse Width (High, Low) | tw | 230 | - | - | |
| | R/W and RS Setup Time | tsu | 40 | - | - | |
| | R/W and RS Hold Time | $t_H$ | 10 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 120 | |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | |

**Table 13. AC Characteristics ($V_{DD}$ =2.7V ~ 4.5V, Ta = -30 ~ +85°C)**

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Fig-6) | E Cycle Time | tc | 1000 | - | - | ns |
| | E Rise / Fall Time | $t_R t_F$ | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | R/W and RS Setup Time | tsu1 | 60 | - | - | |
| | R/W and RS Hold Time | $t_{H1}$ | 20 | - | - | |
| | Data Setup Time | tsu2 | 195 | - | - | |
| | Data Hold Time | $t_{H2}$ | 10 | - | - | |
| Read Mode (Refer to Fig-7) | E Cycle Time | tc | 1000 | - | - | ns |
| | E Rise / Fall Time | $t_R$,$t_F$ | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | R/W and RS Setup Time | tsu | 60 | - | - | |
| | R/W and RS Hold Time | $t_H$ | 20 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 360 | |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | |

**Table 14. AC Characteristics ($V_{DD}$ =2.7V ~ 4.5V, Ta = -30 ~ +85°C)**

| Mode | Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Interface Mode with Extension Driver (Refer to Fig-8) | Clock Pulse Width (High, Low) | tc | 800 | - | - | ns |
| | Clock Rise / Fall Time | $t_R$,$t_F$ | - | - | 25 | |
| | Clock Setup Time | tsu1 | 500 | - | - | |
| | Data Setup Time | tsu2 | 300 | - | - | |
| | Data Hold Time | $t_{DH}$ | 300 | - | - | |
| | M Delay Time | $t_{DM}$ | -1000 | - | 1000 | |

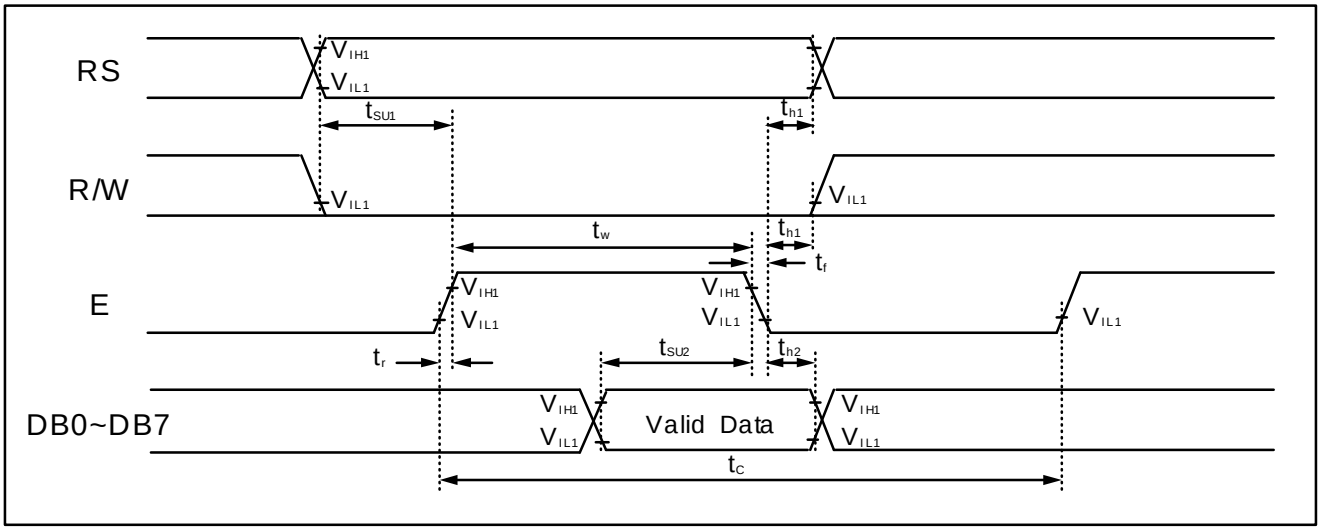



**Figure 6 . Write Mode Timing Diagram**

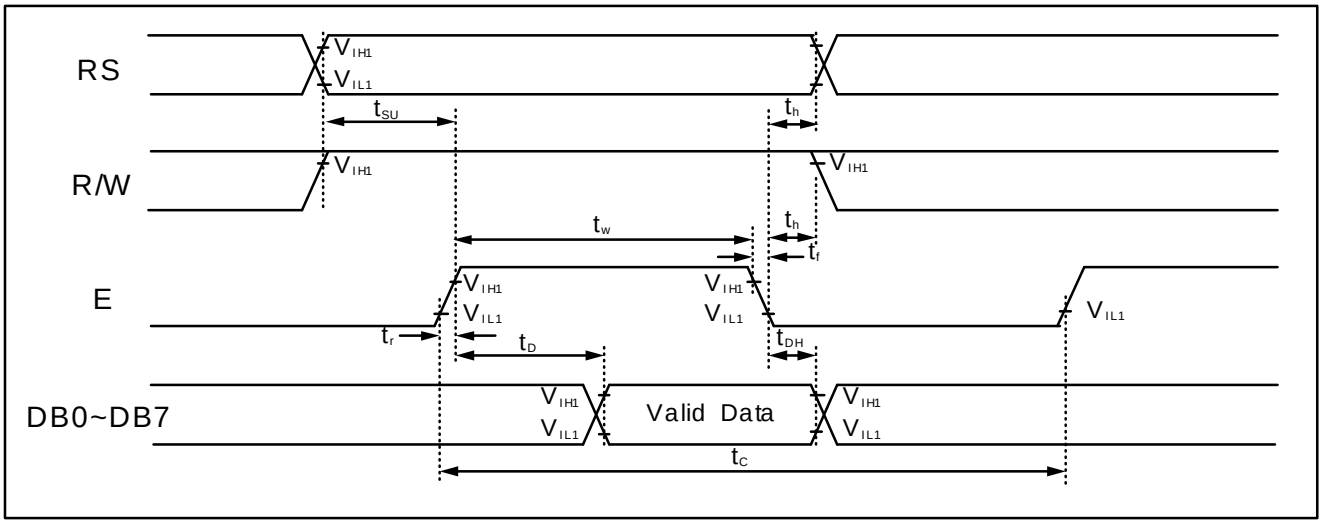



**Figure 7 . Read Mode Timing Diagram**

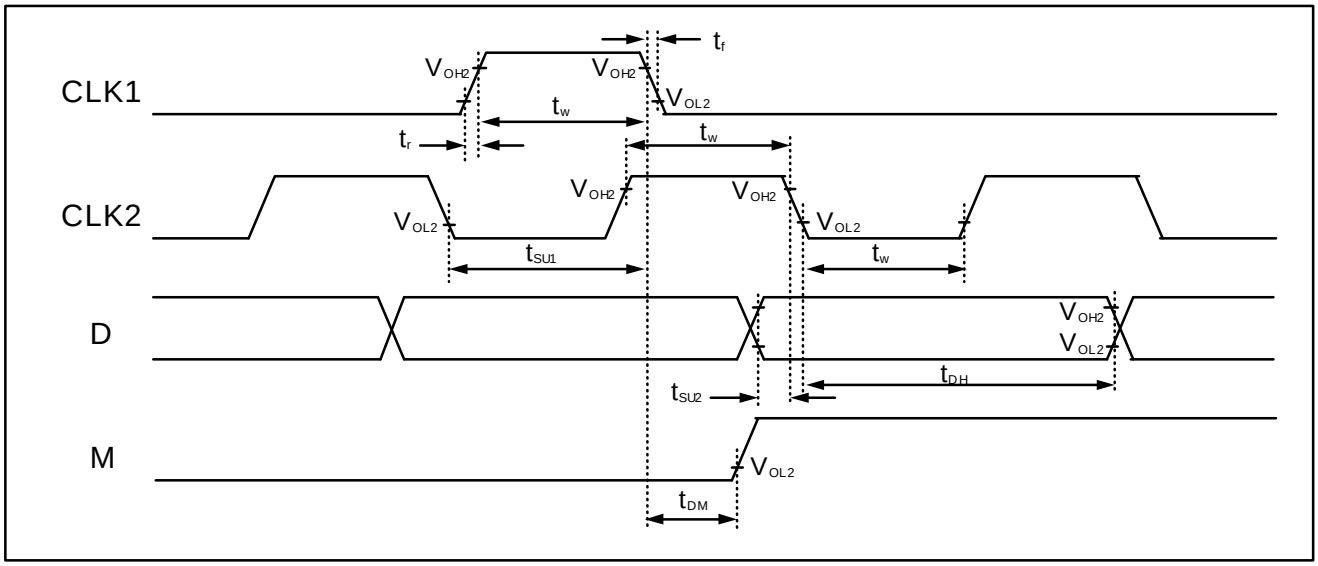
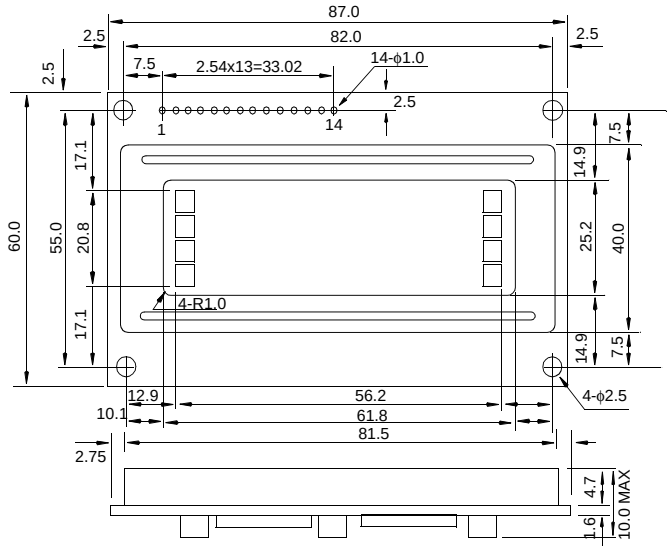


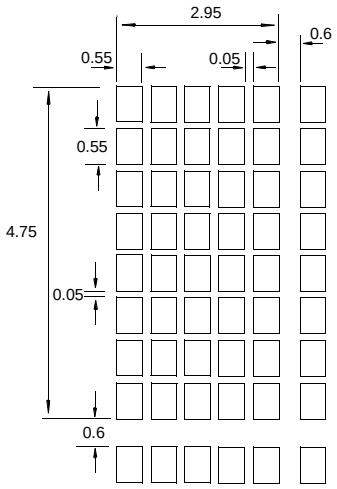

**Figure 8 . Interface Mode With Extension Driver Timing Diagram**

# HDM16416H

16 Character x 4 Lines

## Dimensional Drawing




Dimension tolerance: +/-0.3mm

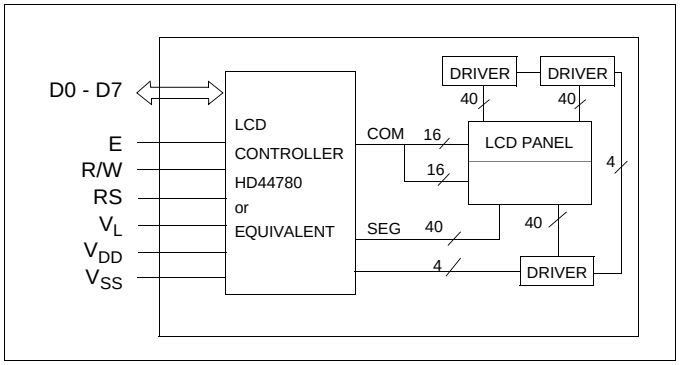
## Features

Character Format .....5x7 Dots with Cursor
Backlight.....EL Optional
Options....TN/Gray STN/Yellow STN, 12 o'Clock/6 o'Clock View
Normal/Extended Temperature
Normal/Negative Displays

## Physical Data

Module Size.....87.0W x 60.0H x 10.0T mm
Viewing Area Size.....61.8W x 25.2H mm
Weight.....45g

## Block Diagram




## Absolute Maximum Ratings

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| SUPPLY VOLTAGE | $V_{DD}$-$V_{SS}$ | 0 | 7.0 | V |
| SUPPLY VOLTAGE FOR LCD | $V_{DD}$-$V_L$ | 0 | 13.5 | V |
| INPUT VOLTAGE | $V_{IN}$ | $V_{SS}$ | $V_{DD}$ | V |
| OPERATING TEMPERATURE | $T_{OP}$ | 0 | 50 | °C |
| STORAGE TEMPERATURE | $T_{STG}$ | -20 | 70 | °C |

## Electrical Characteristics (VDD=5.0±0.25V 25°C)

| PARAMETER | SYM | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| INPUT HIGH VOLTAGE | $V_{IH}$ | - | 2.2 | - | - | V |
| INPUT LOW VOLTAGE | $V_{IL}$ | - | - | - | .06 | V |
| OUTPUT HIGH VOLTAGE | $V_{OH}$ | $I_{OH}$=0.2mA | 2.4 | - | - | V |
| OUTPUT LOW VOLTAGE | $V_{OL}$ | $I_{OL}$=1.2mA | - | - | 0.4 | V |
| POWER SUPPLY CURRENT | $I_{DD}$ | $V_{DD}$=5.0V | - | 1.0 | 2.2 | mA |
| POWER SUPPLY FOR LCD | $V_{DD}$-$V_L$ | TA=25°C | 4.3 | - | 4.7 | V |
| DRIVE METHOD | 1/16 Duty | | | | | |

## Pin Connections

| PIN NO. | SYMBOL | LEVEL | FUNCTION | |
|---|---|---|---|---|
| 1 | $V_{SS}$ | - | 0V | Power supply |
| 2 | $V_{DD}$ | - | 5V | |
| 3 | $V_L$ | - | - | |
| 4 | RS | H/L | H: Data input<br>L: Instruction data input | |
| 5 | R/W | H/L | H: Data read<br>L: Data write | |
| 6 | E | H,H→L | Enable signal | |
| 7 | D0 | H/L | Data bus | |
| 8 | D1 | H/L | | |
| 9 | D2 | H/L | | |
| 10 | D3 | H/L | | |
| 11 | D4 | H/L | | |
| 12 | D5 | H/L | | |
| 13 | D6 | H/L | | |
| 14 | D7 | H/L | | |